# FE-I Overview and Schedule

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## FE-I Overview:

- Two vendor design approach
- Goals of FE-I design

## FE-I Schedule:

- Test Chip program using TSMC as a quick-turn
- Milestones on the way to the IBM engineering run submission

# Design Approach

## Presently have access to 0.25μ process from two vendors:

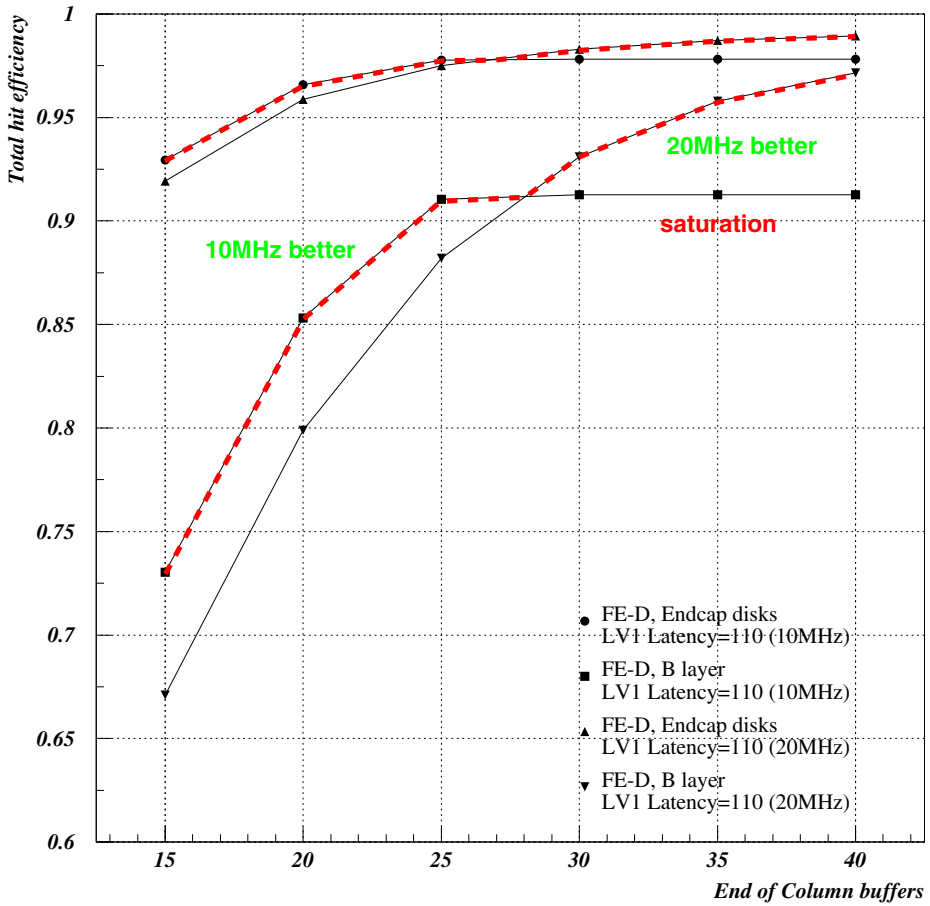
- IBM CMOS6SF process, available through CERN frame contract. CERN organized MPW runs about 3 times per year for 3-metal designs. Engineering runs (2-6 wafers, 13 week turnaround) and Production runs (48-... wafers, 20 week turnaround) available at any time. Prices and terms guaranteed through Mar. 2004 under contract.
- TSMC CL25 process, available through MOSIS consortium. Now support monthly submissions in both 0.25μ and 0.18μ process, with 8-10 week turnaround. Dedicated runs also available, and could probably purchase several hundred wafers per year in this way (almost production volume).

## Have decided to pursue a common design and layout:

- Slightly modified design rules, and a few other tricks, allow common layout for both processes (final mods done on the fly when GDS streamed out). Process parameters very similar for digital design, differences are more significant for analog design. However, large corners for IBM largely cover differences.
- Will hear about progress in this direction from Gerrit and Mario today.

# Goals of FE-I Design

- Start with geometry and buffering achieved in the HSOI design of 400μ pixel and 32 EOC buffers. New design should work at 2.0V for extra margin, and would start from FE-H pinout.
- Design copes with needs except for B-layer point resolution (300μ pixel preferred) and high efficiency at high luminosity for the B-layer (more buffering needed).




Study of D. Calvet indicating expected efficiency for hits (not clusters) versus number of buffers and column clock frequency.

Four basic sources of loss are: analog (TOT deadtime), digital (pixel readout busy), buffering (no free EOC buffer), and fakes (hits arriving in EOC too late for L1).

For 20MHz and 32 buffers, dominant source is available buffers, and this can be improved by increasing the buffer count still further to about 40.

## Necessary changes for 0.25μ conversion include:

- Revised front-end design driven by lack of small W/L NMOS devices for enclosed layouts, and reduced supply voltage. Most likely requires different leakage compensation scheme and two-stage design, possibly providing better timewalk.

## Basic improvements planned for design include:

- Improved threshold control with replacement of V-DACs and possible trimming of feedback current at pixel level for improved TOT and timewalk performance.
- Improved SEU tolerance of configuration registers and logic blocks.
- Fully static design of all logic and storage blocks for improved leakage and SEU performance (and possibly yield).
- Improved performance of pixel RAM and sense amplifiers.
- Improved robustness of basic logic blocks in readout path (pixel hit logic, CEU logic, EOC logic) via more synchronous state-machine-based designs.
- Increase number of TSI bits from 7 to 8 for increased latency range (even number of bits is natural in the layout).

## More ambitious improvements to investigate:

- Investigate differential front-end design for improved common mode immunity.
- Investigate possibility of computing TOT in CEU and applying simply timing correction for timewalk at this stage.

# Test Chip Program

## Take advantage of frequent runs, rapid turnaround of TSMC:

- Earliest date for useful submission is Jan 8, with expected return of Mar 19.
- Goal of the initial submission is to include several of basic blocks from FE-I, and evaluate their performance.
- Gives opportunity to check that we understand design rules, that performance agrees with SPICE, and that behavior during irradiation (SEU) and post-rad (total dose) is as expected.

## Present list of blocks includes:

- Current reference and current DAC used in bias control
- Redesigned LVDS driver and receiver blocks
- Pixel RAM block with sense amplifier readout
- Several basic shift registers, for evaluation of SEU performance. Designs will include: standard cell version, SEU-tolerant version, and three-fold majority logic version.
- Basic digital block which has been synthesized and automatically placed and routed.

## Progress towards submission on Jan 8 date looks good.

# Next step should be more complete test chip:

- This would naturally be something like the Analog Test Chip included in FE-D runs. This included several short column-pair arrays of preamp/discriminator and bias circuitry, with all adjustment DACs and calibration circuitry, and real layout.
- It would allow us to demonstrate that the front-end design and all of the analog blocks intended for FE-I do indeed behave as expected.
- A submission on Feb 5, with return about Apr 16, would allow time to evaluate the results and make minor adjustments to the design if needed. If more significant issues were uncovered, the engineering run would have to be delayed.

# Milestones in overall schedule:

- Schematics should be largely completed by early February
- Layout should be largely completed by early March
- Simulation and verification would then have almost three months to complete
- Submission would be June 1. In order to get the guaranteed turnaround, the design would need to be DRC-clean, requiring us to begin foundry-level DRC checking (using Hercules) at least several weeks earlier.
- Worst case thirteen week turnaround in the frame contract would give wafers during the first week in September. This might allow some testbeam and irradiation studies at CERN before shutdowns in early November...